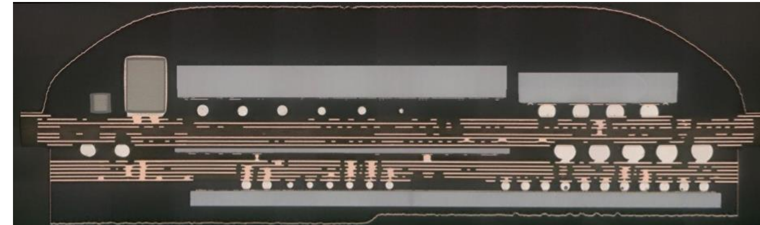


Source:
Highly Integrated 3D-SiP:
Apple AirPods Pro,
Cross-Section by System
Plus Consulting 2019

Overview ESPAT-Consulting

European Semiconductor
Packaging, Assembly and Test

JUN/23, 2021

Dresden, Germany

Introduction ESPAT-Consulting

European Semiconductor Packaging, Assembly and Test (ESPAT)
Consultancy Services Offer:

- **Packaging Technology** decision-making for new applications/products (Start-ups, SME);
- **Package Design**, Bill of Material (BOM) and Process of Record (POR) support;
- **Supply Chain** setup for prototypes, samples, small-medium-high volume manufacturing;
- **Technology Promotion** for innovative SPAT technology development companies;
- **Strategic Guidance** provision to SPAT equipment and material suppliers on what's next;
- **Technology Trend** analysis for Market Studies and Technology Reports;
- **Market Researchers** and Trend Scouting support;
- **Research Institutes** cooperation on national and European project acquisition;
- **Active Representation** of European SPAT in relevant international industry associations:
    - SEMI Europe - APC Chair @ SEMICON Europa, Founder & Vice Chair of ESiPAT-TC;
    - IEEE Electronics Packaging Society (EPS) - Elected to BoG 2021-2023 for Region 8 (EMEA);
    - IMAPS (Europe, US) - Conference Program Committee Member, and SMTA.

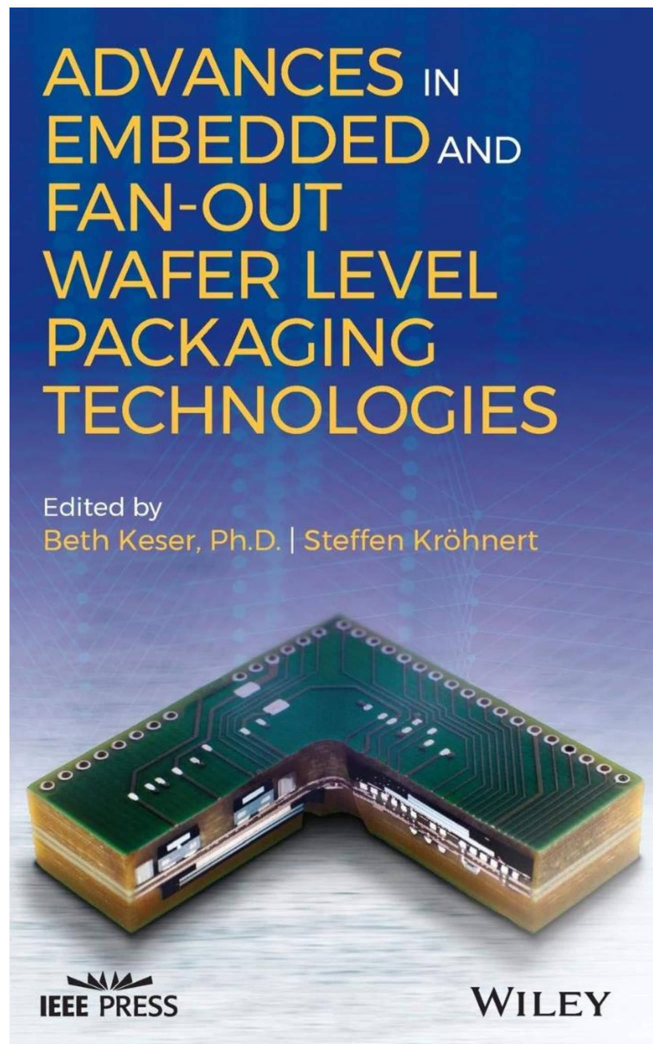
Background Steffen Kröhnert

TSOP → FBGA → AdvPkg/SiP/HI/ WLP/FOWLP →

Chemnitz Hatfield (UK) Reutlingen Regensburg Dresden Porto Dresden/Porto Dresden - LOCATION -

1991 1997 1999 2002 2006 2010 2012 2017 2018 2019 2020 - YEAR -

Recommended Reading by the Co-Editor



Examines the advantages of Embedded and FO-WLP technologies, potential application spaces, package structures available in the industry, process flows, and material challenges

Embedded and fan-out wafer level packaging (FO-WLP) *technologies* have been developed across the industry over the past 15 years and have been in high volume manufacturing for nearly a decade. This book covers the advances that have been made in this new packaging technology and discusses the many benefits it provides to the electronic packaging industry and supply chain. It provides a compact overview of the major types of technologies offered in this field, on what is available, how it is processed, what is driving its development, and the pros and cons.

Filled with contributions from some of the field's leading experts, *Advances in Embedded and Fan-Out Wafer Level Packaging Technologies* begins with a look at the history of the technology. It then goes on to examine the biggest technology and marketing trends. Other sections are dedicated to chip-first FO-WLP, chip-last FO-WLP, embedded die packaging, materials challenges, equipment challenges, and resulting technology fusions. This valuable text:

- Discusses specific company standards and their development results
- Relates its content to practice as well as to contemporary and future challenges in electronics system integration and packaging

Advances in Embedded and Fan-Out Wafer Level Packaging Technologies will appeal to microelectronic packaging engineers, managers, and decision makers working in OEMs, IDMs, IFMs, OSATs, silicon foundries, materials suppliers, equipment suppliers, and CAD tool suppliers. It is also an excellent book for professors and graduate students working in microelectronic packaging research.

Beth Keser, Ph.D., is a recognized global leader in the semiconductor industry with over 20 years' experience resulting in 28 patents and patents pending and over 40 publications. She is an IEEE Senior Member whose volunteer activities and professional society responsibilities include: IEEE EPS' VP of Education, 2015 ECTC General Chair, and more.

Steffen Kröhnert, M.Sc., is Senior Director of Technology Development at Amkor Technology Holding B.V., Germany. He has more than 20 years' experience in the semiconductor industry. Steffen is author and co-author of 23 patent filings in the area of Semiconductor Packaging Technology, and an active member of IEEE EPS, IMAPS, SMTA, VDI, VDE and GPM.

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<u>2nd book in progress</u>:

"Embedded and Fan-Out Wafer and Panel Level Packaging Technologies for Advanced Application Spaces: High Performance Compute and System-in-Package"

Publishing Date: May 2022

Thanks for your attention !